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10/058,264	01/29/2002	Koji Tomioka	NEC01P260-HYa	4190

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EXAMINER	
NGUYEN, THUONG	

ART UNIT	PAPER NUMBER
2455	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/058,264	TOMIOKA, KOJI	
	Examiner	Art Unit	
	Thuong T. Nguyen	2455	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,10-12,14-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8, 10-12,14-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to application 10/058,264 the amendment filed on 10/27/09. Claims 2-8, 10-12, 14-20, 22-24 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-8, 10-12, 14-20, 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingam, Patent No. 6,205,503 in view of Christensen, Patent No. 6,742,136 B2.

4. As to claim 2, Mahalingam teaches a computer system comprising:

a plurality of central processing unit (CPU) and memory installed apparatus comprising a CPU and a memory (Mahalingam, figure 2; col 4, lines 28-65; i.e., plurality of computer processors which comprised CPU, I/O and memory) ;

a plurality of input/output control apparatus which are assigned to the plurality of CPU and memory installed apparatus, respectively, and communicate with the plurality of CPU and memory installed apparatus via a network (Mahalingam, figure 3; col 7, lines 34-57; i.e., peripheral devices communicate and connect to each other through a LAN); and

wherein a CPU and memory installed apparatus of said plurality of CPU and memory installed apparatus comprises communication means for transmitting an input/output instruction issued by a CPU of the CPU and memory installed apparatus to an input/output control apparatus assigned to said CPU and memory installed apparatus via said network, and receives a response from said input/output control apparatus via said network (Mahalingam, figure 2; col 4, lines 28-50; col 7, lines 59-65; i.e., CPUs, memories and I/O devices communicate with each other via network),

wherein said input/output control apparatus comprises communication means for receiving the input/output instruction from the CPU and memory installed apparatus assigned to said input/output control apparatus via said network, and transmits a response to said input/output instruction to said CPU and memory installed apparatus via said network (Mahalingam, figure 2; col 4, lines 28-50; col 5, lines 65 - col 6, lines 15; i.e., CPUs, memories and I/O devices communicate via network), and

But Mahalingam failed to teach the claim limitation wherein a plurality of diagnostic control circuits which are connected to the plurality of the CPU and memory installed apparatus and said plurality of input/output control apparatus; said plurality of diagnostic control circuits comprises a diagnostic control circuit connected to the CPU and memory installed apparatus and input/output control apparatus, and if said diagnostic control circuit detects a fault in the CPU and memory installed apparatus, then the diagnostic control circuit determines an other CPU and memory installed apparatus of the plurality of CPU and memory installed apparatus which will use the input/output control apparatus.

However, Christensen teaches the limitation wherein a plurality of diagnostic control circuits which are connected to the plurality of the CPU and memory installed apparatus and said plurality of input/output control apparatus (Christensen, figure 1; col 5, lines 30-47; col 18, lines 45-55; i.e., establishing the relationship between the redundant I/O devices, process control network, the active I/O device and the backup I/O devices); said plurality of diagnostic control circuits comprises a diagnostic control circuit connected to the CPU and memory installed apparatus and input/output control apparatus, and if said diagnostic control circuit detects a fault in the CPU and memory installed apparatus, then the diagnostic control circuit determines an other CPU and memory installed apparatus of the plurality of CPU and memory installed apparatus which will use the input/output control apparatus (Christensen, col 13, lines 49-66; col 15, lines 24-56; i.e., to detect the connection port or slot or the configuration of the allocated connection or removed connection).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mahalingam in view of Christensen so that the system would be able to diagnosed CPU group, main memory access controller and IOP group. One would be motivated to do so to provide a control networks that seamlessly and transparently takes over for the disabled primary I/O device without disrupting the implementation process (see Christensen, col 2, lines 37-61).

5. As to claim 3, Mahalingam and Christensen teach a computer system as recited in claim 2, wherein means for receiving the input/output instruction as being effective only when the source of the input/output instruction received via said network is a CPU

and memory installed apparatus which has been set in advance (Mahalingam, col 7, lines 59-65; i.e., configured the setting in advanced).

6. As to claim 4, Mahalingam and Christensen teach a computer system as recited in claim 2, wherein means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatus which has been set in advance (Mahalingam, figure 2; col 8, lines 10-15; i.e., allows the system to access the elements only when the memory has been configured in advance).

7. As to claim 5, Mahalingam and Christensen teach a computer system as recited in claim 2, wherein said CPU and memory installed apparatus communicates with other CPU and memory installed apparatuses in said plurality of CPU and memory installed apparatuses via said network (Mahalingam, figure 2; col 4, lines 28-65; i.e., plurality of computer processors which comprised CPU, I/O and memory).

8. As to claim 7, Mahalingam and Christensen teach a computer system as recited in claim 5, wherein means for communicating with other CPU and memory installed apparatus via said network (Mahalingam, figure 3; col 7, lines 34-57; i.e., peripheral devices communicate and connect to each other through a LAN).

9. As to claim 8, Mahalingam and Christensen teach a computer system as recited in claim 7, wherein the communications between said CPU and memory installed apparatus and the other CPU and memory installed apparatuses comprise communications for accessing memories installed on the other CPU and memory

installed apparatuses (Mahalingam, figure 2; col 4, lines 28-65; i.e., plurality of computer processors which comprised CPU, I/O and memory).

10. As to claim 10, Mahalingam and Christensen teach a computer system as recited in claim 2, wherein the other CPU and memory installed apparatus comprises an active one of the CPU and memory installed apparatus which is using another input/output control apparatus (Mahalingam, figure 5; col 10, lines 3-13; i.e., keeping track of the configured information for all the elements).

11. As to claim 11, Mahalingam and Christensen teach a computer system as recited in claim 2, wherein a backup CPU and memory installed apparatus, said backup CPU and memory installed apparatus being used as said other CPU and memory installed apparatus (Mahalingam, col 4, lines 33-50; i.e., using the secondary processor in case of the failure in the system).

12. As to claim 12, Mahalingam and Christensen teach a computer system as recited in claim 2, wherein a backup input/output control apparatus which is assigned to the CPU and memory installed apparatus if the input/output control apparatus is faulty (Mahalingam, col 11, lines 5-17; i.e., freeze and restart communication to a specified adapter once detected the failure).

13. As to claim 14, Mahalingam teaches a CPU and memory installed apparatus comprising:

at least one central processing unit (CPU) and at least one memory (Mahalingam, figure 2; col 4, lines 28-65; i.e., plurality of computer processors which comprised CPU, I/O and memory);

communication means for communicating with an external circuit comprising an input/output control apparatus, transmitting an input/output instruction issued by said CPU to said input/output control apparatus which has been assigned in advance, and receiving a response from said input/output control apparatus (Mahalingam, figure 2 & 6; col 4, lines 28-50; col 7, lines 59-65; i.e., CPUs, memories and I/O devices communicate with each other via network).

But Mahalingam failed to teach the claim limitation wherein a diagnostic control circuit connected with said CPU and said at least one memory and with said input/output control apparatus; a single board on which said CPU, said memory, said diagnostic control circuit and said communication means are mounted; said diagnostic control circuit detects a fault in said CPU and memory installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between an other non-faulty CPU and memory installed apparatus in the computer system and the input/output control apparatus.

However, Christensen teaches the limitation wherein a diagnostic control circuit connected with said CPU and said at least one memory and with said input/output control apparatus (Christensen, figure 1; col 5, lines 30-47; col 18, lines 45-55; i.e., establishing the relationship between the redundant I/O devices, process control network, the active I/O device and the backup I/O devices); a single board on which said CPU, said memory, said diagnostic control circuit and said communication means are mounted (Christensen, figure 6 & 8; i.e., backplane for implementing the redundant bus I/O devices); said diagnostic control circuit detects a fault in said CPU and memory

installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between an other non-faulty CPU and memory installed apparatus in the computer system and the input/output control apparatus (Christensen, col 13, lines 49-66; col 15, lines 24-56; i.e., to detect the connection port or slot or the configuration of the allocated connection or removed connection).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mahalingam in view of Christensen so that the system would be able to diagnosed CPU group, main memory access controller and IOP group. One would be motivated to do so to provide a control networks that seamlessly and transparently takes over for the disabled primary I/O device without disrupting the implementation process (see Christensen, col 2, lines 37-61).

14. As to claim 16, Mahalingam teaches an input/output control apparatus for a computer system, said apparatus comprising:

an input/output control circuit for controlling a peripheral device based on an input/output instruction (Mahalingam, figure 2; col 4, lines 28-65; i.e., plurality of computer processors which comprised CPU, I/O and memory); and

communication means for communicating with an external circuit comprising a central processing unit (CPU) and memory installed apparatus and memory installed apparatus which has been set in advance and transferring said input/output instruction to said input/output control circuit, and for transmitting a response to said input/output instruction to said CPU and memory installed apparatus (Mahalingam, figure 2 & 6; col

4, lines 28-50; col 7, lines 59-65; i.e., CPUs, memories and I/O devices communicate with each other via network).

But Mahalingam failed to teach the claim limitation wherein at least one diagnostic control circuit, for receiving an input/output instruction from said CPU; wherein if said diagnostic control circuit detects a fault in said CPU and memory installed apparatus, said diagnostic control circuit retrieve previously stored information that determines a new connection between an other non-faulty CPU and memory installed apparatus in the computer system and the input/output control apparatus.

However, Christensen teaches the limitation wherein at least one diagnostic control circuit, for receiving an input/output instruction from said CPU (Christensen, figure 1; col 5, lines 30-47; col 18, lines 45-55; i.e., establishing the relationship between the redundant I/O devices, process control network, the active I/O device and the backup I/O devices); wherein if said diagnostic control circuit detects a fault in said CPU and memory installed apparatus, said diagnostic control circuit retrieve previously stored information that determines a new connection between an other non-faulty CPU and memory installed apparatus in the computer system and the input/output control apparatus (Christensen, col 13, lines 49-66; col 15, lines 24-56; i.e., to detect the connection port or slot or the configuration of the allocated connection or removed connection).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mahalingam in view of Christensen so that the system would be able

to diagnosed CPU group, main memory access controller and IOP group. One would be motivated to do so to provide a control networks that seamlessly and transparently takes over for the disabled primary I/O device without disrupting the implementation process (see Christensen, col 2, lines 37-61).

15. As to claim 18, Mahalingam and Christensen teach a computer system as recited in claim 2, wherein each of said plurality of input/output control apparatus further comprises an input/output (I/O) device (Mahalingam, figure 2; col 4, lines 28-65; i.e., plurality of computer processors which comprised CPU, I/O and memory).

16. As to claim 19, Mahalingam and Christensen teach a computer system as recited in claim 18, wherein said input/output (I/O) device is connected to a peripheral device (Mahalingam, col 4, lines 65 – col 5, lines 3; i.e., connecting the devices to a peripheral device).

17. As to claim 20, Mahalingam and Christensen teach a computer system as recited in claim 18, wherein said input/output (I/O) device is connected to a second network (Mahalingam, figure 6; i.e., including different LAN classes).

18. As to claim 22, Mahalingam and Christensen teach a computer system as recited in claim 2, wherein said communication means comprises a plurality of ports (Mahalingam, figure 1; i.e., including plurality of controllers and adapters).

19. As to claim 23, Mahalingam and Christensen teach a computer system as recited in claim 22, wherein each of said plurality of input/output control apparatus is allocated to at least one of said plurality of ports of said communication means (Mahalingam, figure 5; i.e., I/O bus, I/O devices, system bus and expansion bus).

20. Claims 6 & 15 are directed to a computer system and memory claims and they do not teach or further define over the limitations recited in claim 4. Therefore, claims 6 & 15 are also rejected for similar reasons set forth in claim 4.

21. Claim 17 is directed to an input/output claim and they do not teach or further define over the limitations recited in claim 3. Therefore, claim 17 is also rejected for similar reasons set forth in claim 3.

22. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingam, Patent No. 6,205,503 in view of Christensen, Patent No. 6,742,136 B2, and further in view of Horst, Patent No. 5,867,501.

23. As to claim 24, Mahalingam and Christensen teach a computer system as recited in claim 22. But Mahalingam and Christensen failed to teach the claim limitation wherein when one of the plurality of CPU and memory installed apparatus stops its operation with one of said plurality of input/output control apparatus, said one of said plurality of input/output control apparatus is newly allocated to any one of the plurality of ports to which said one of said plurality of input/output control apparatus was not previously allocated.

However, Horst teaches the limitation wherein when one of the plurality of CPU and memory installed apparatus stops its operation with one of said plurality of input/output control apparatus, said one of said plurality of input/output control apparatus is newly allocated to any one of the plurality of ports to which said one of said

plurality of input/output control apparatus was not previously allocated (Horst, col 4, lines 48 – col 5, lines 28; i.e.,).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mahalingam in view of Christensen so that the system would be able to determine the fault elements and disconnected that element from the groups. One would be motivated to do so to improve the response time, latency affects service levels and employee productivity (see Horst, col 4, lines 32-38).

Response to Arguments

Applicant's arguments with respect to claims 1, 14 & 16 have been considered but are moot in view of the new ground(s) of rejection. Applicant's arguments include the failure of previously applied art to expressly disclose a plurality of input/output control apparatus which are assigned to the plurality of CPU and memory installed apparatus, respectively, and communicate with the plurality of CPU and memory installed apparatus via a network (see Applicant's response, 10/27/09, page 11, paragraph 3). It is evident from the detailed mappings found in the above rejection(s) that Mahalingam disclosed this functionality (see Mahalingam, figure 2-3; col 4, lines 28-65; col 7, lines 34-57; i.e., peripheral devices communicate and connect to each other through a LAN and plurality of computer processors which comprised CPU, I/O and memory). Further, it is clear from the numerous teachings (previously and currently cited) that the provision for said plurality of diagnostic control circuits comprises a diagnostic control circuit connected to the CPU and memory installed apparatus and input/output control

apparatus, and if said diagnostic control circuit detects a fault in the CPU and memory installed apparatus, then the diagnostic control circuit determines an other CPU and memory installed apparatus of the plurality of CPU and memory installed apparatus which will use the input/output control apparatus was widely implemented in the networking art. Thus, Applicant's arguments drawn toward distinction of the claimed invention and the prior art teachings on this point are not considered persuasive.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuong T. Nguyen whose telephone number is (571)272-3864, and the fax number is 571-273-3864. The examiner can normally be reached on 9:00AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on 571-272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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